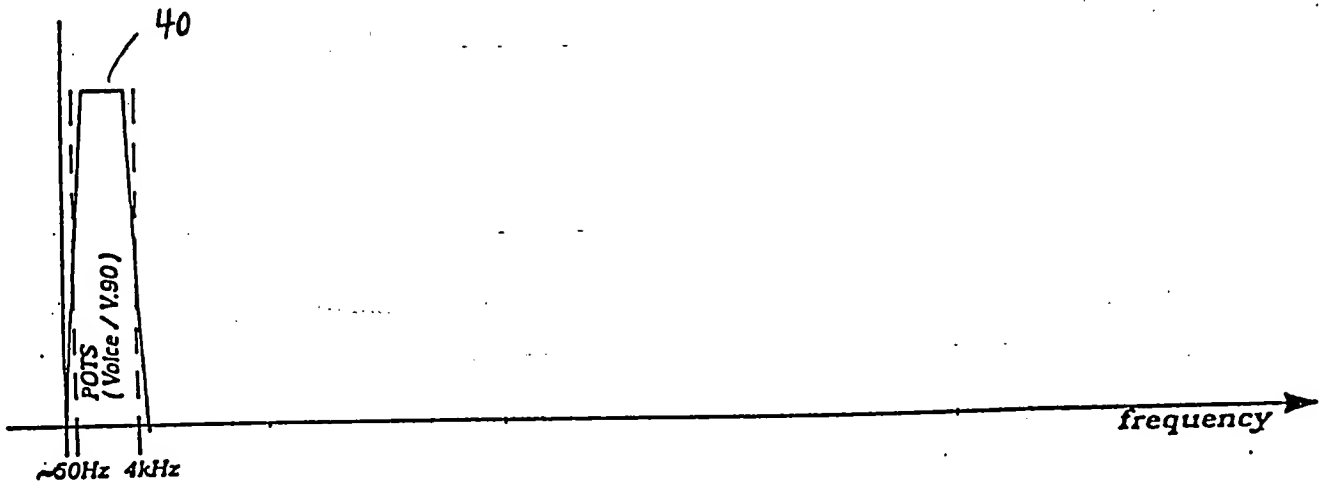

Fig 1 Prior Art

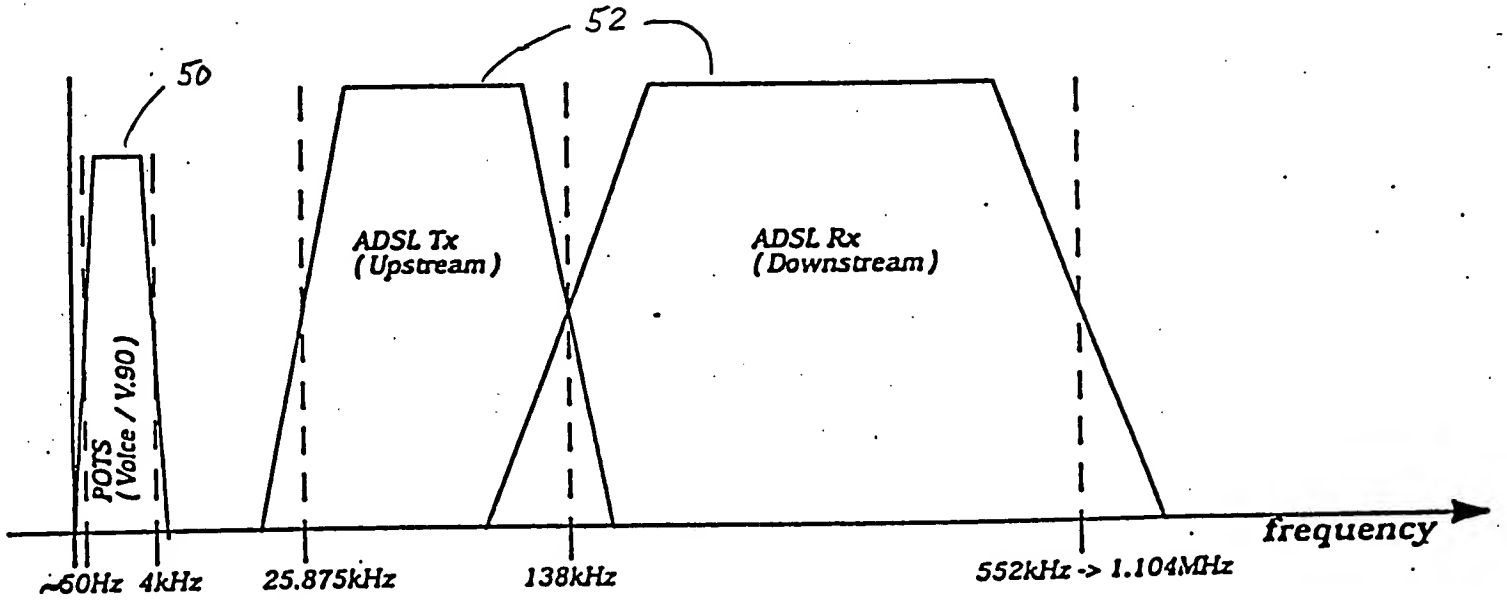

Fig 2

Prior Art

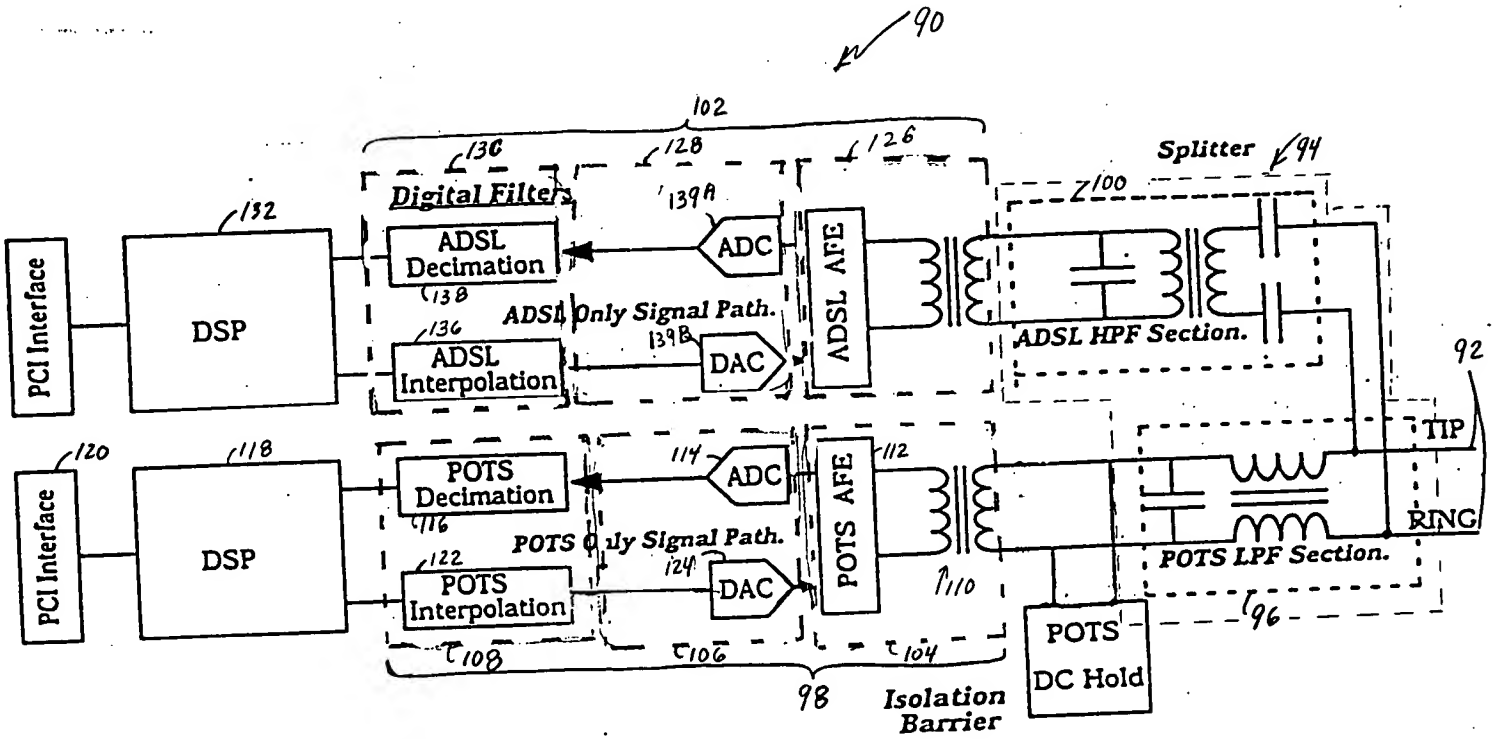

Fig. 3 Prior Art

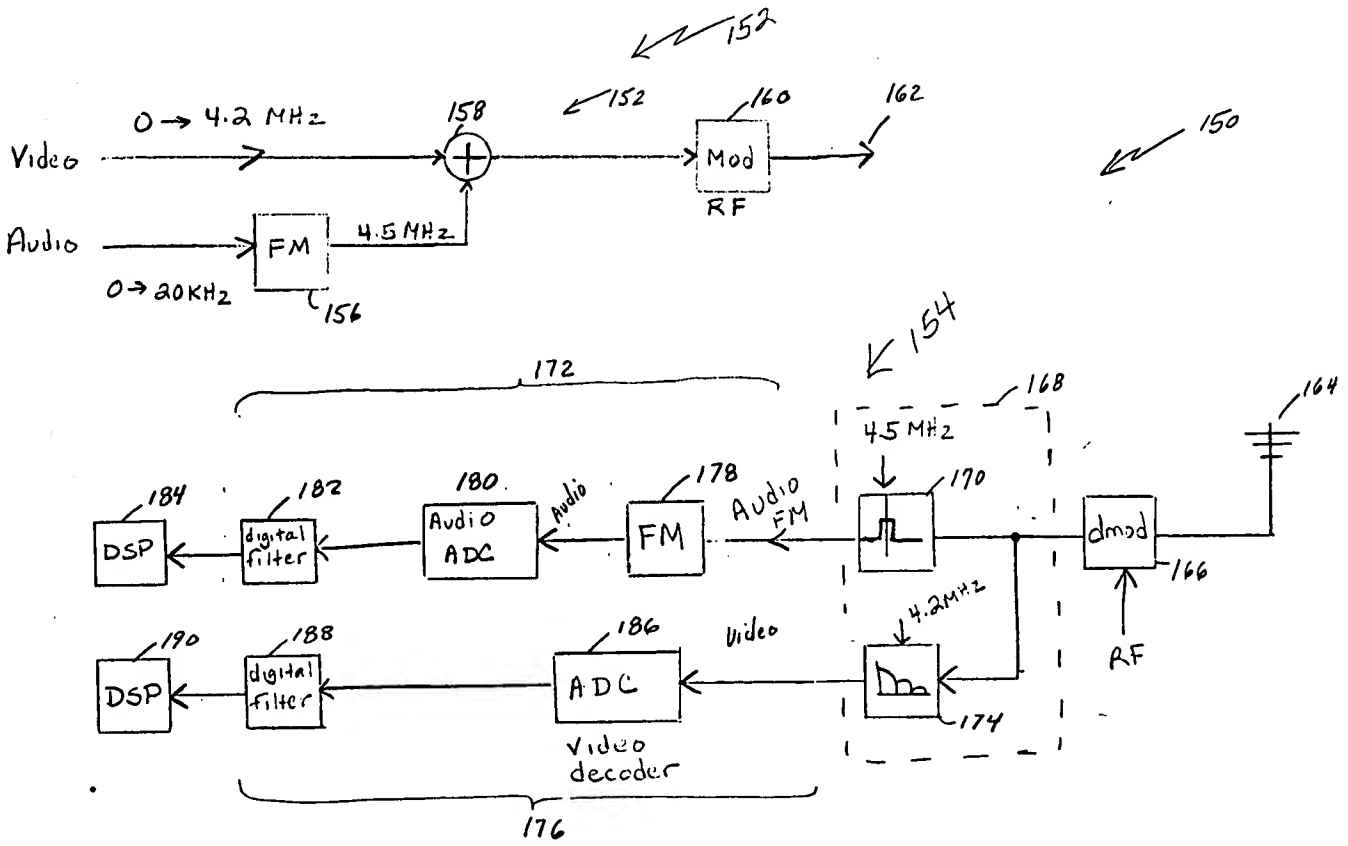

Fig 4 Prior Art

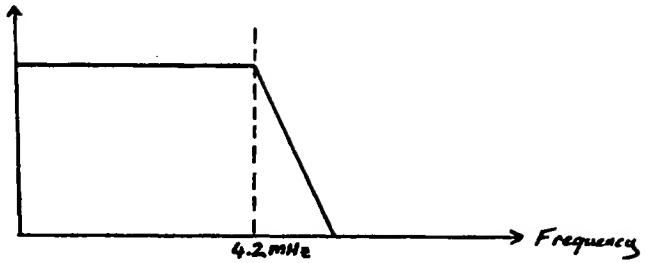

Fig. 5 Prior Art

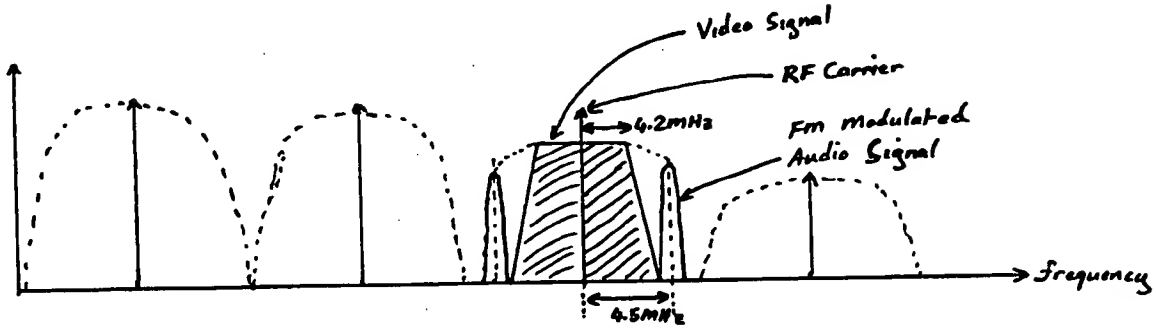

Fig 6 Prior Art

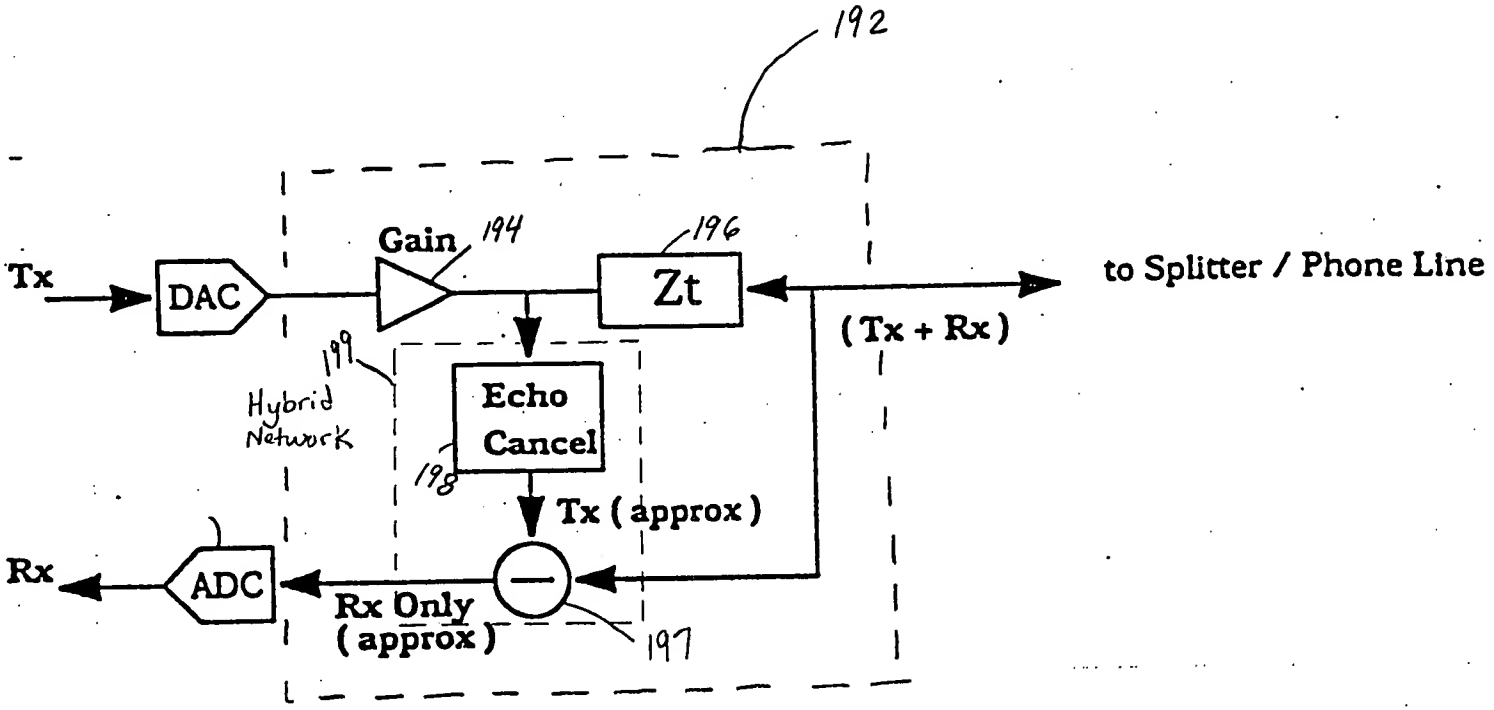

Fig. 7 Prior Art

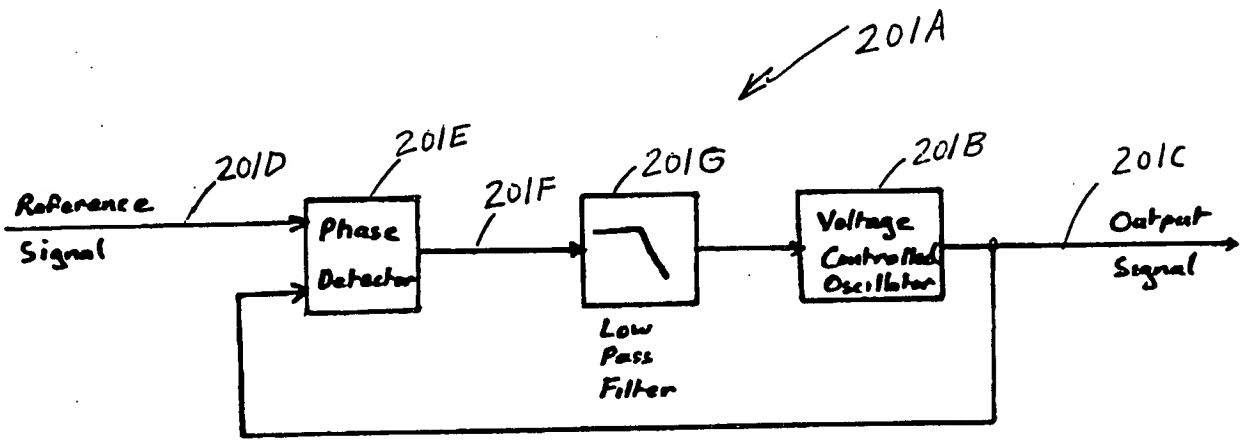

Fig 8 Prior Art

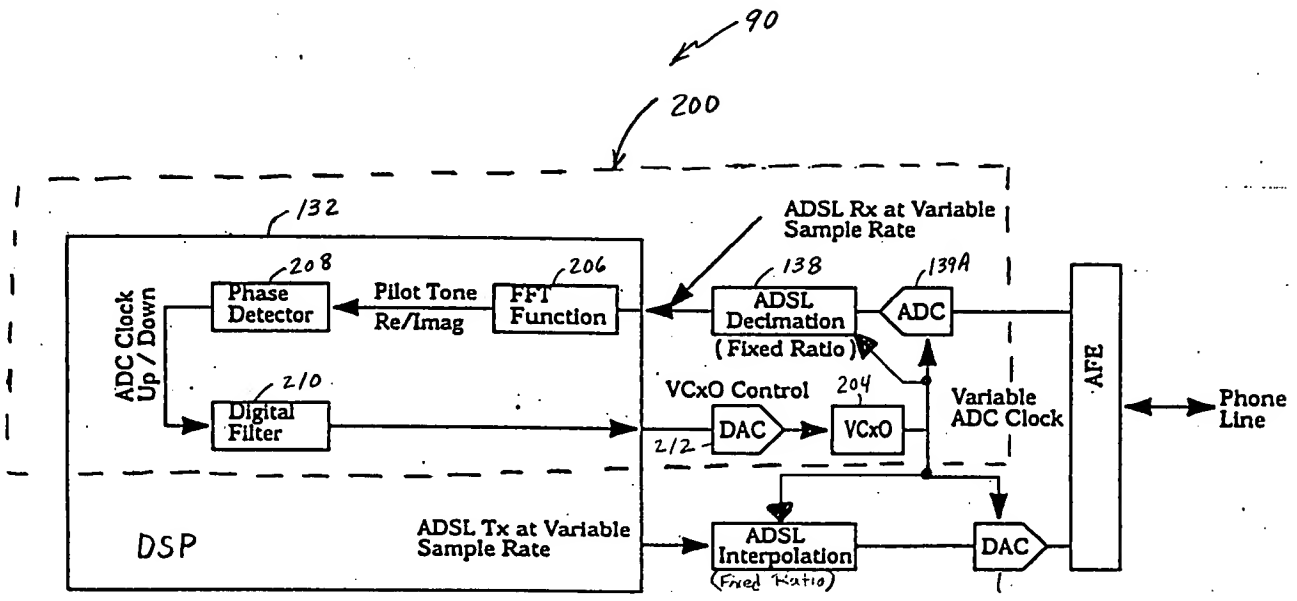

Fig. 9 Prior Art

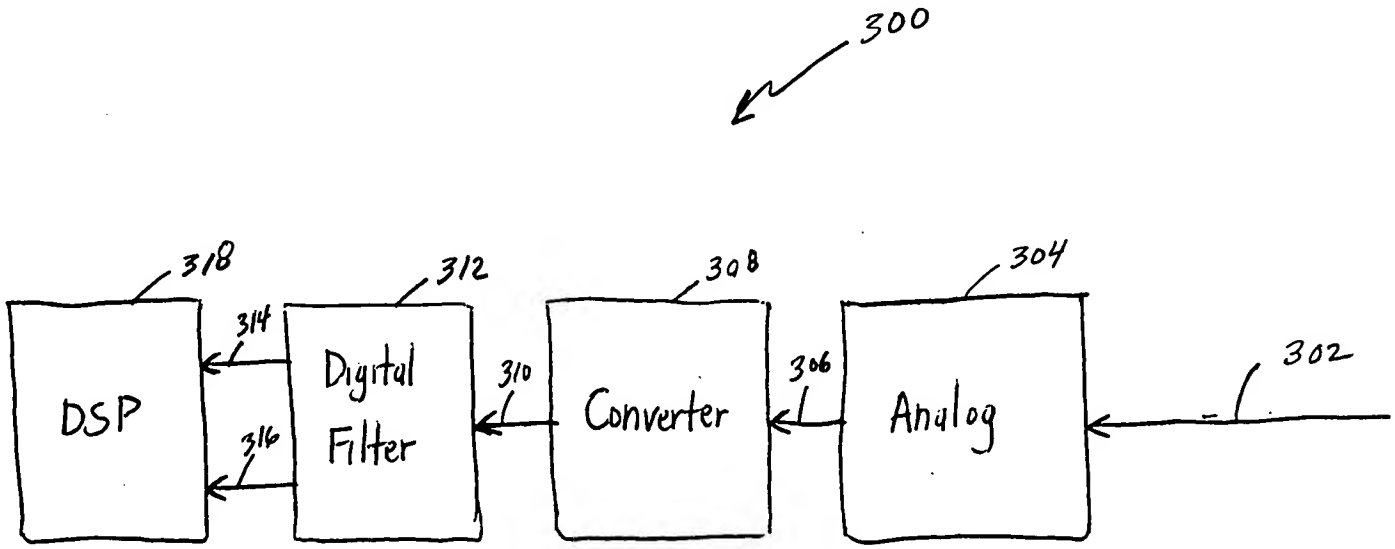

Fig. 10

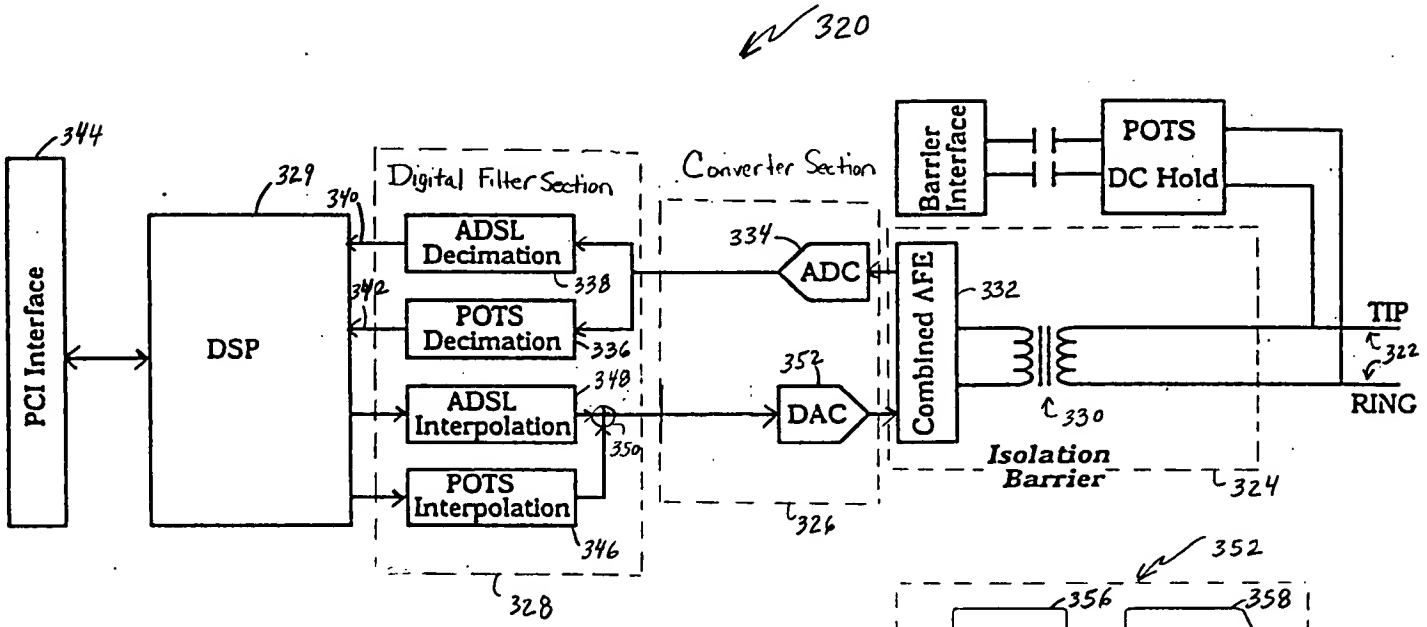

Fig. 11a

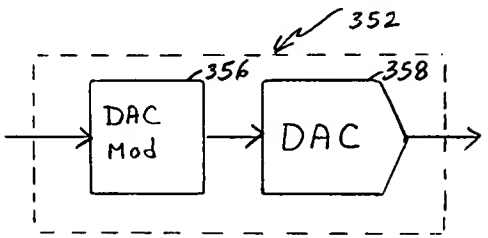

Fig. 11b

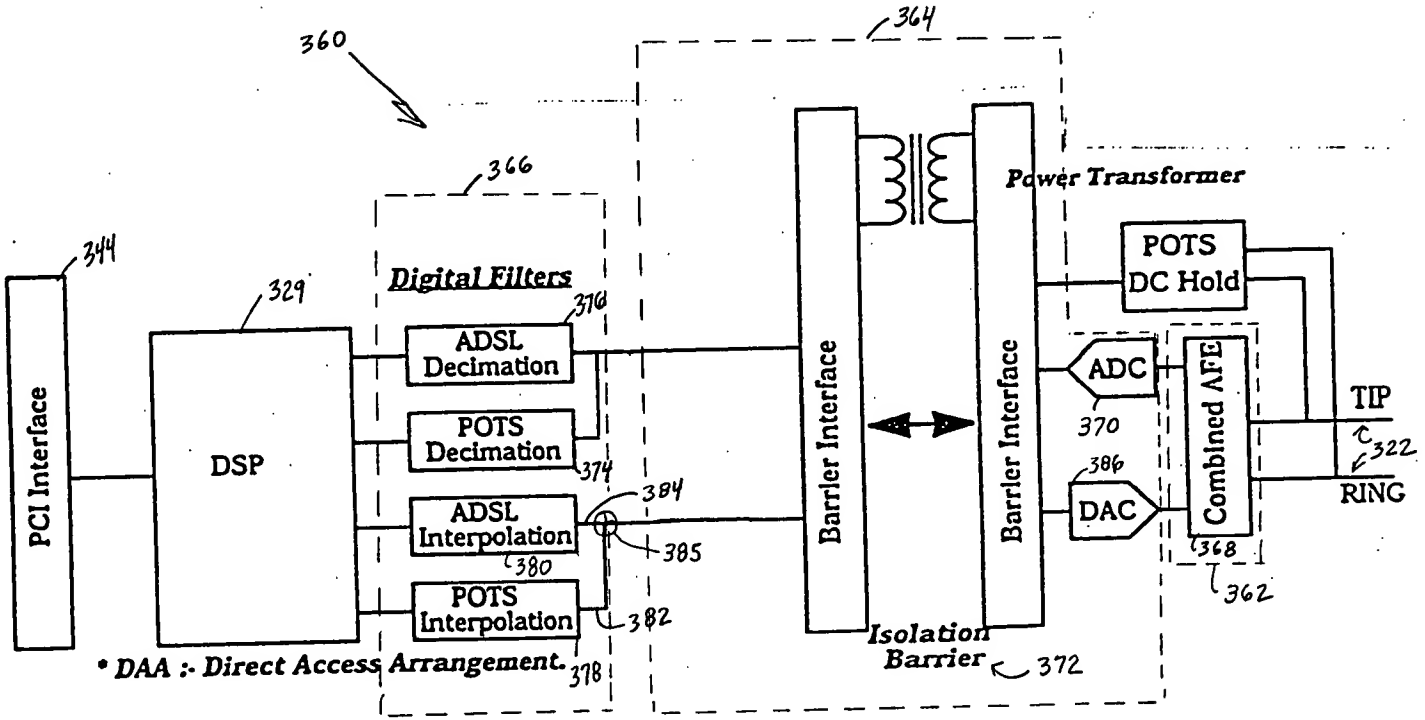

Fig. 12a

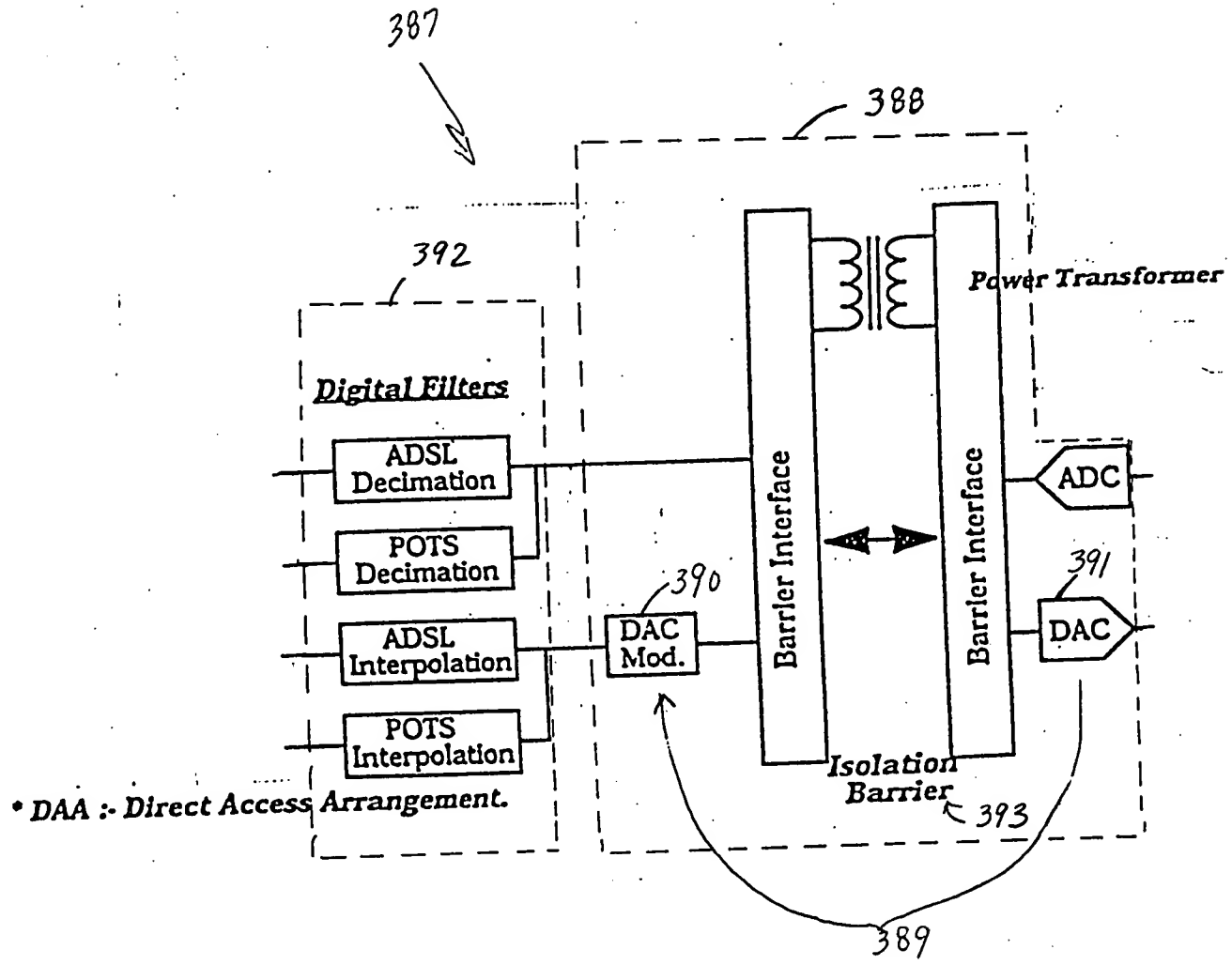
387
388
392
Digital Filters
ADSL Decimation
POTS Decimation
ADSL Interpolation
POTS Interpolation
390
DAC Mod.
Barrier Interface
Barrier Interface
Power Transformer
ADC
391
DAC
Isolation Barrier
393
389
• DAA :- Direct Access Arrangement.

Fig. 12b

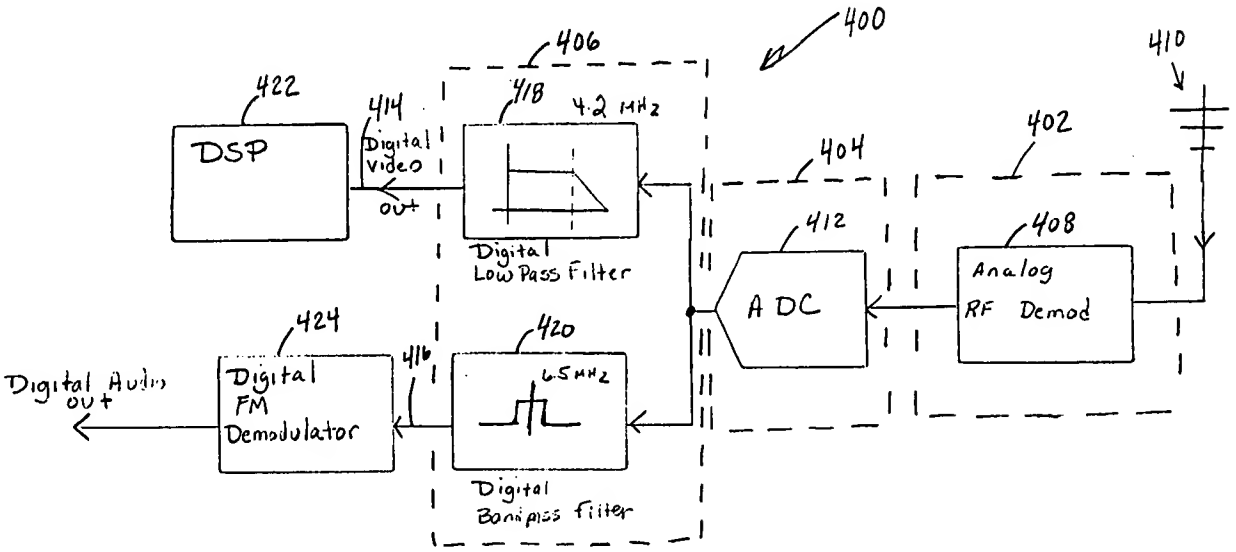

Fig. 13

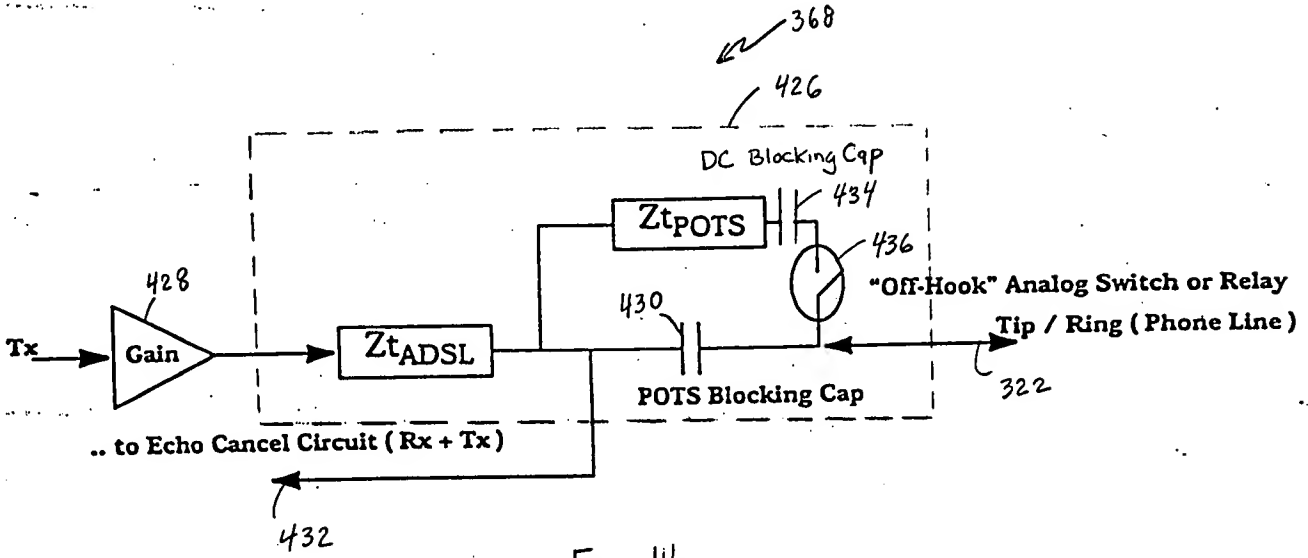
368
426
DC Blocking Cap
434
Zt_{POTS}
436
"Off-Hook" Analog Switch or Relay
428
430
Tx
Gain
Zt_{ADSL}
Tip / Ring (Phone Line)
322
POTS Blocking Cap
.. to Echo Cancel Circuit (Rx + Tx)
432

Fig. 14a

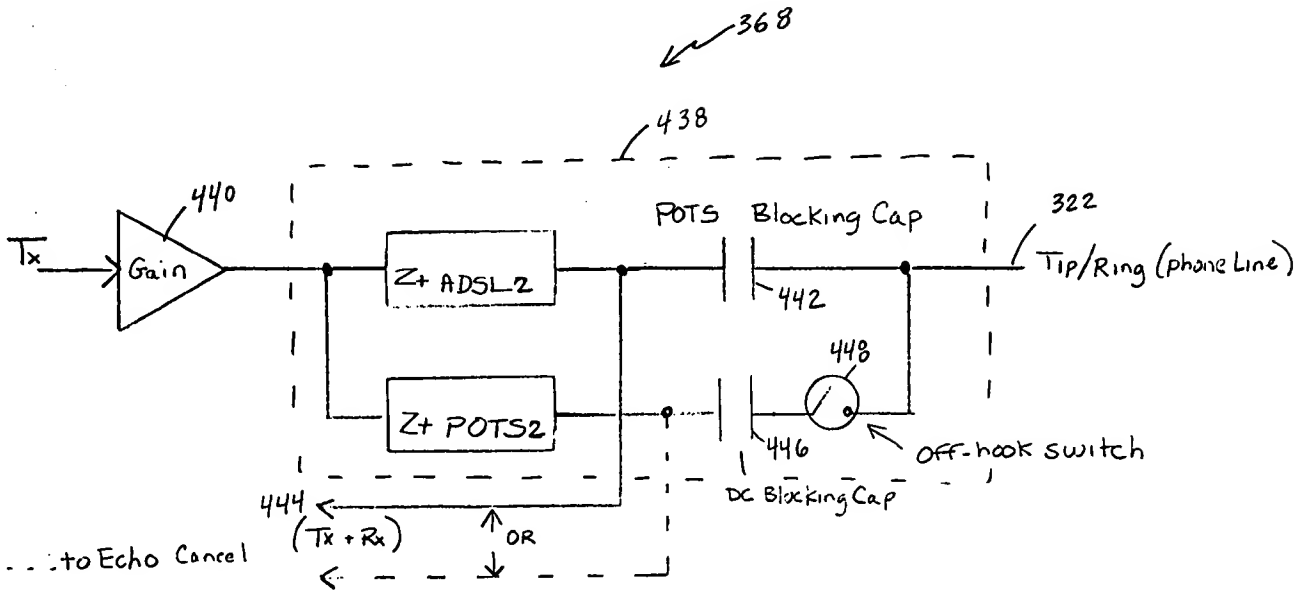

Fig 14b

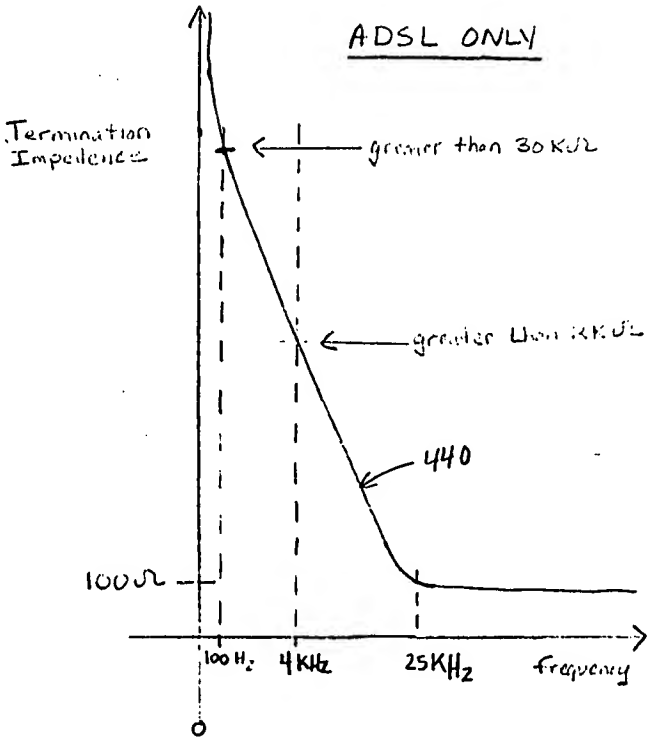

Fig. 15a

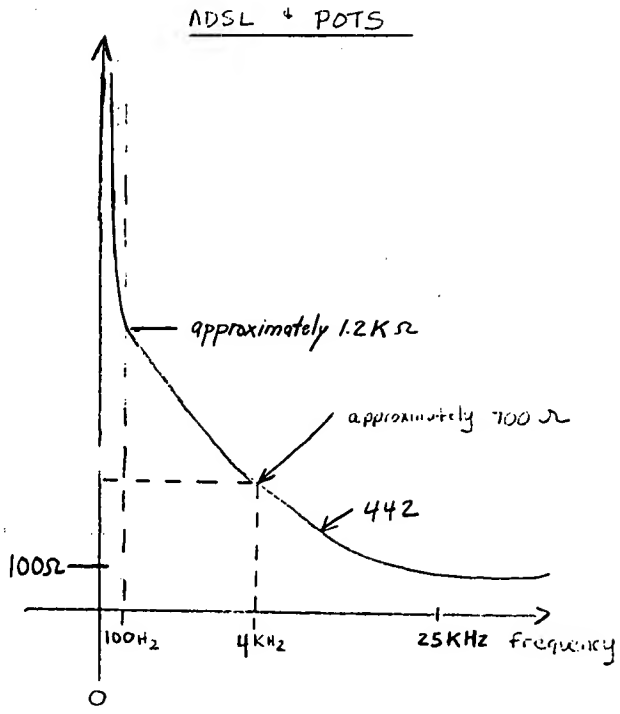

Fig. 15b

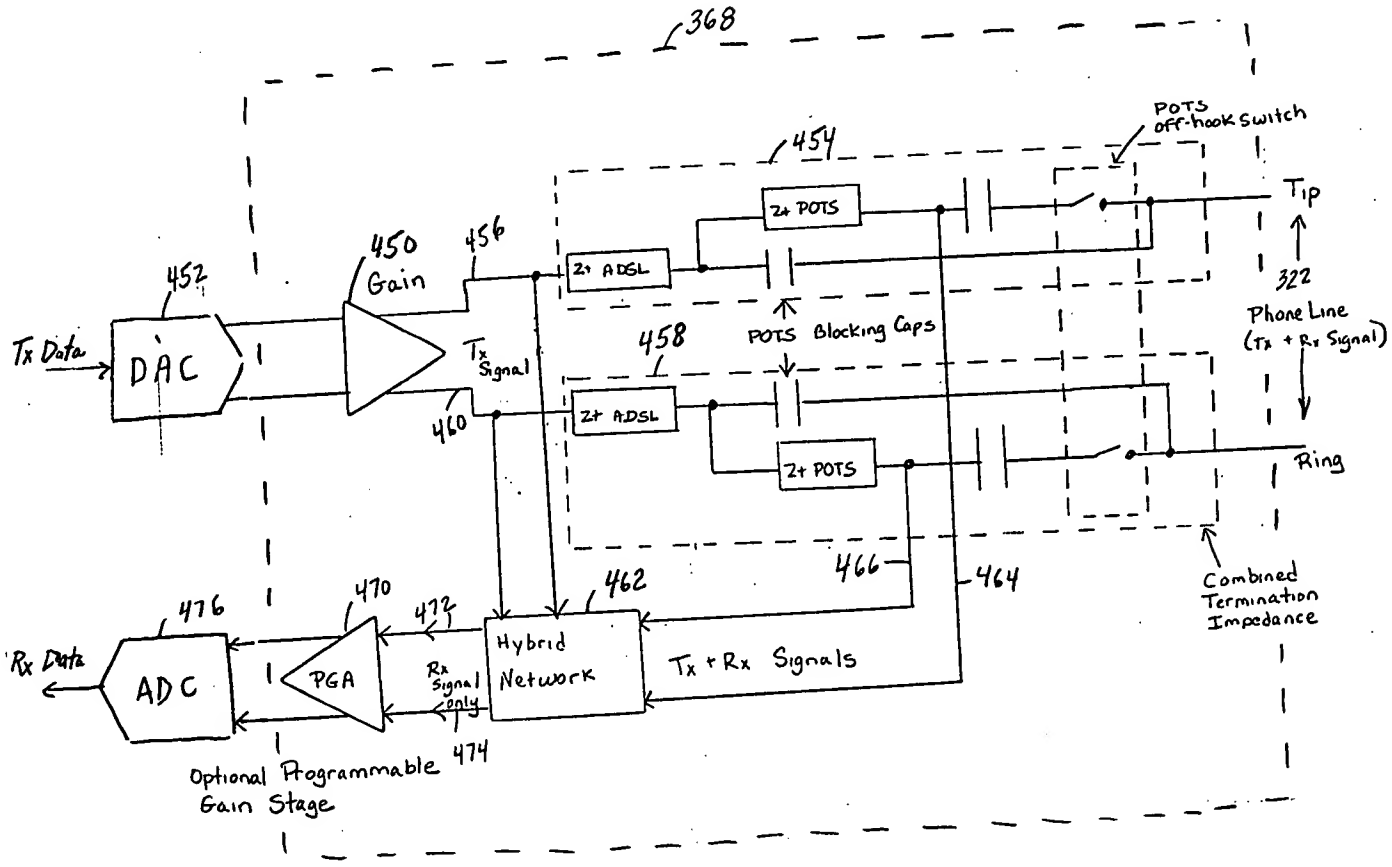

Fig 16a

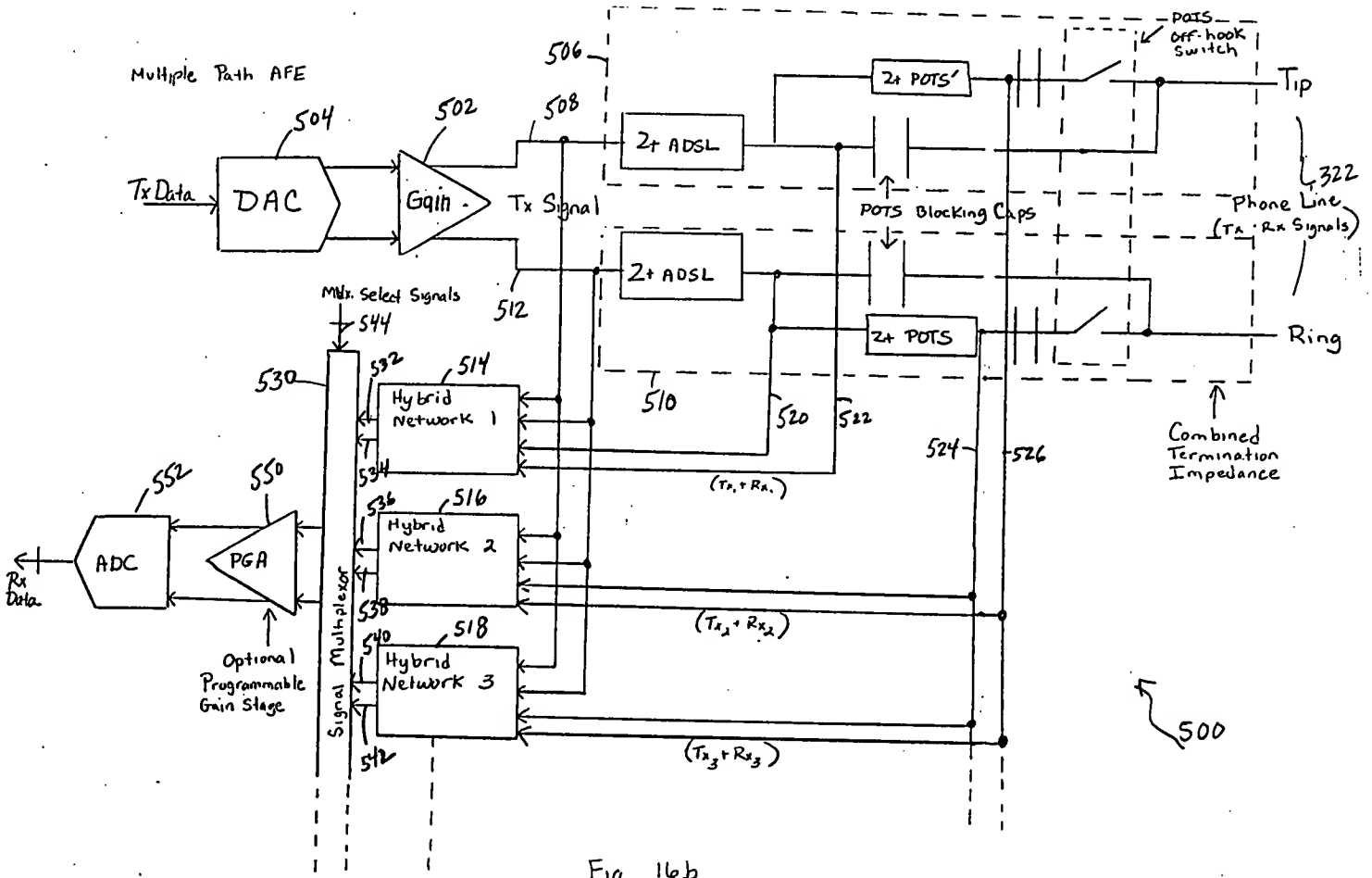

Fig 16b

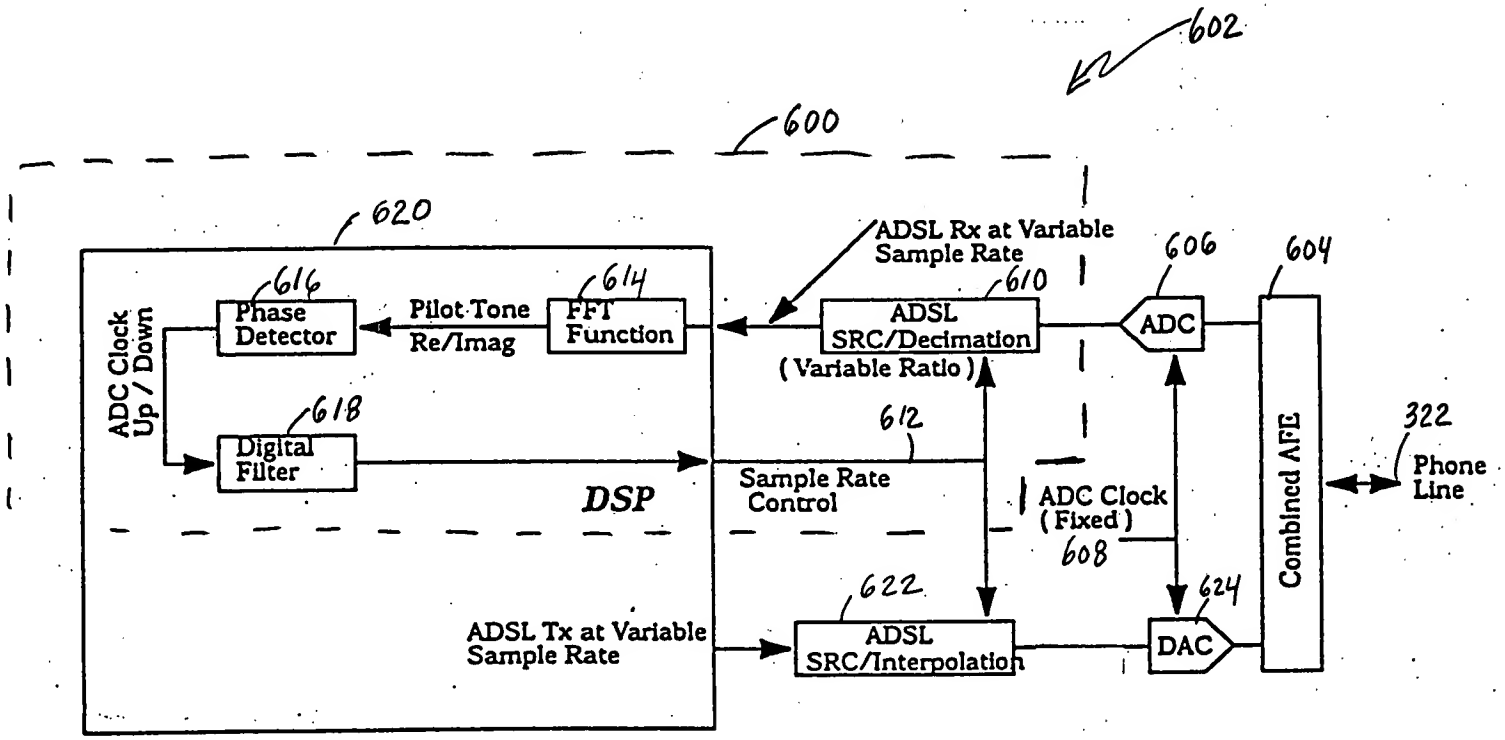

Fig. 17

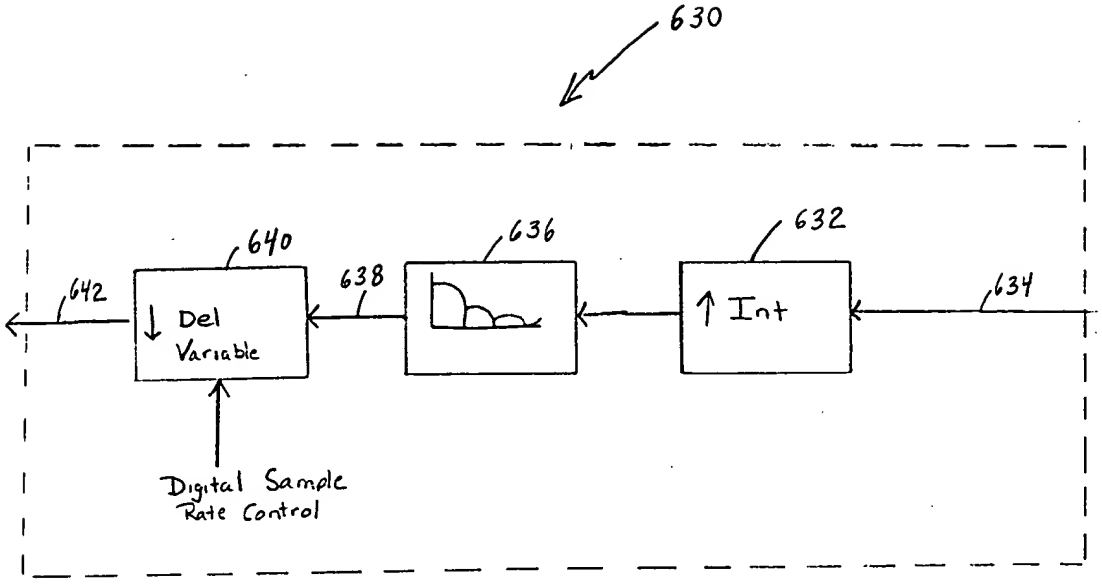
630
640
636
632
642
638
634
↓ Del
Variable
↑ Int
Digital Sample
Rate Control

Fig 18

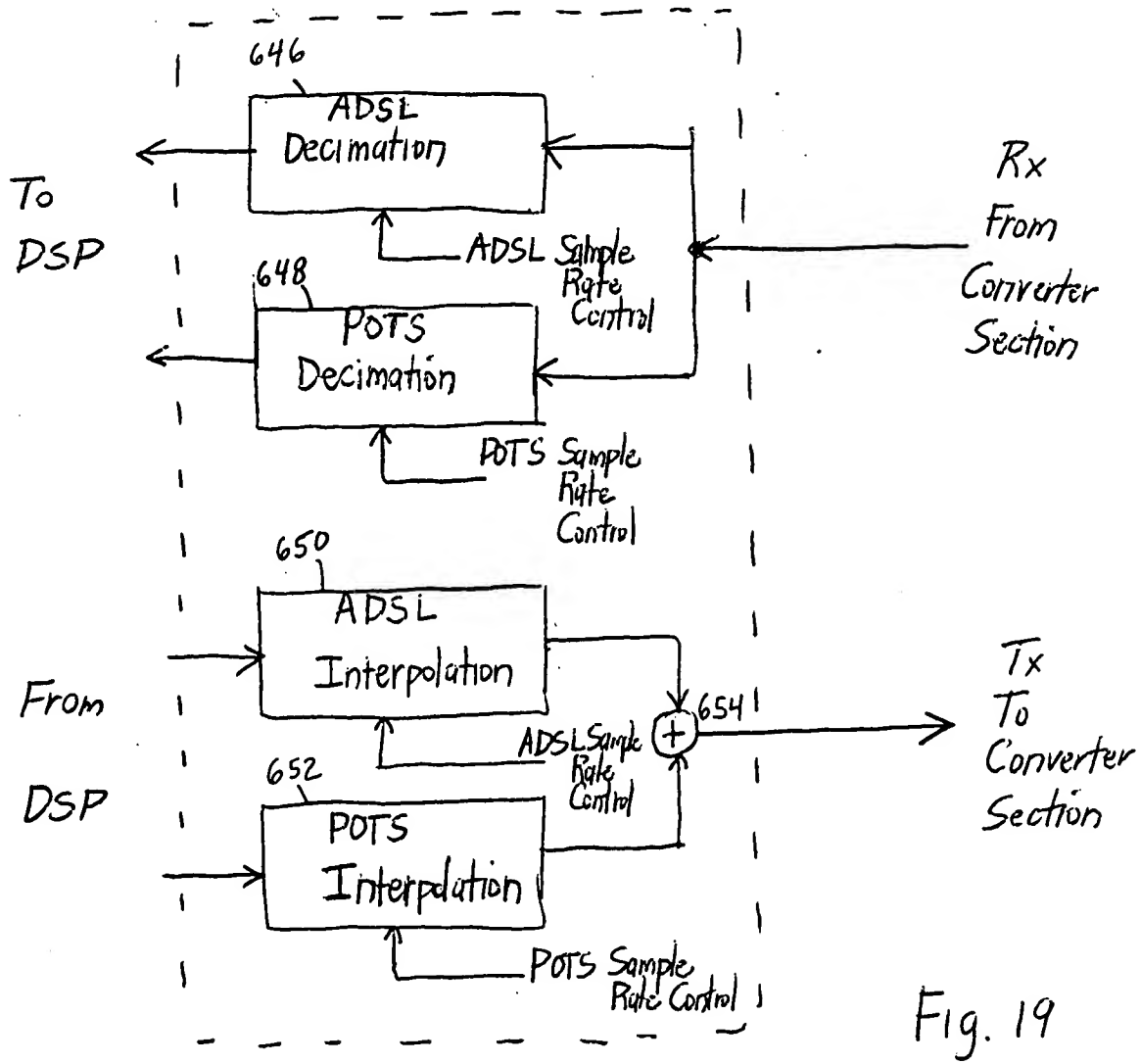
646
ADSL Decimation
To DSP
ADSL Sample Rate Control
Rx From Converter Section
648
POTS Decimation
POTS Sample Rate Control
650
ADSL Interpolation
From DSP
654
Tx To Converter Section
ADSL Sample Rate Control
652
POTS Interpolation
POTS Sample Rate Control

Fig. 19

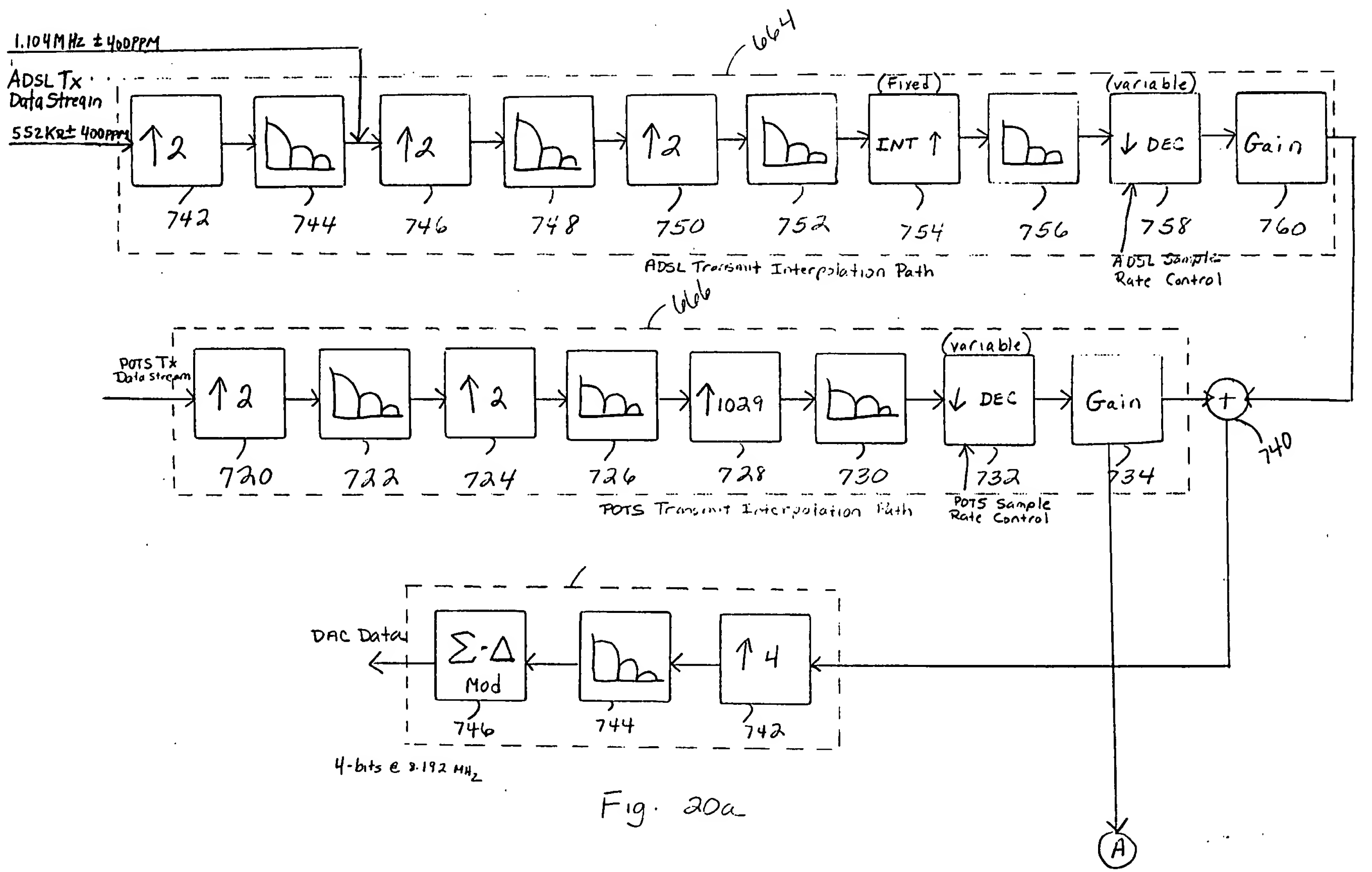
1.104MHz ± 400PPM
ADSL Tx Data Stream
552KHz ± 400PPM
↑2
742
744
↑2
746
748
↑2
750
752
(Fixed)
INT ↑
754
756
(variable)
↓ DEC
758
Gain
760
ADSL Sample Rate Control
ADSL Transmit Interpolation Path
664
666
POTS Tx Data Stream
↑2
720
722
↑2
724
726
↑1029
728
730
(variable)
↓ DEC
732
Gain
734
POTS Sample Rate Control
POTS Transmit Interpolation Path
+
740
A
↑4
742
744
Σ-Δ Mod
746
DAC Data
4-bits @ 8.192 MHz

Fig. 20a

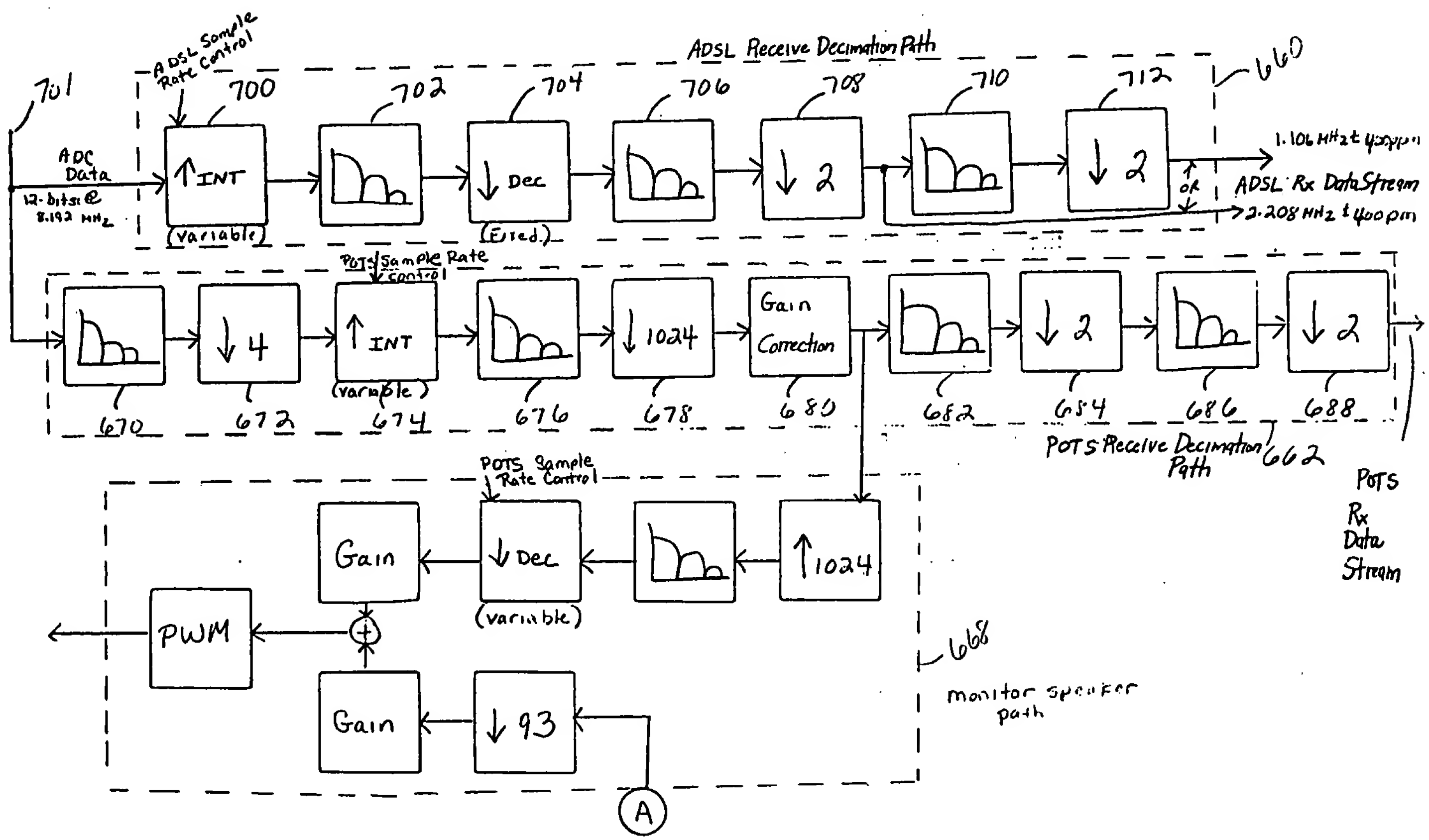
701
ADC Data
12-bits @ 8.192 MHz
ADSL Sample Rate Control
700
INT
(Variable)
702
704
Dec
(Fixed)
706
708
↓2
710
712
↓2
660
ADSL Receive Decimation Path
1.106 MHz ± 400ppm
or
ADSL Rx Data Stream
2.208 MHz ± 400ppm
POTS Sample Rate Control
670
↓4
672
INT
(variable)
674
676
↓1024
678
Gain Correction
680
682
↓2
684
686
↓2
688
POTS Receive Decimation Path
662
POTS Rx Data Stream
POTS Sample Rate Control
↑1024
Dec
(variable)
Gain
PWM
Gain
↓93
A
668
monitor speaker path

Fig 20b

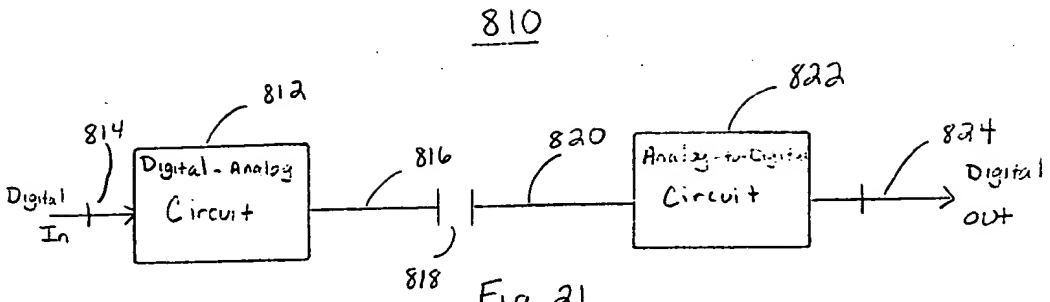

Fig. 21

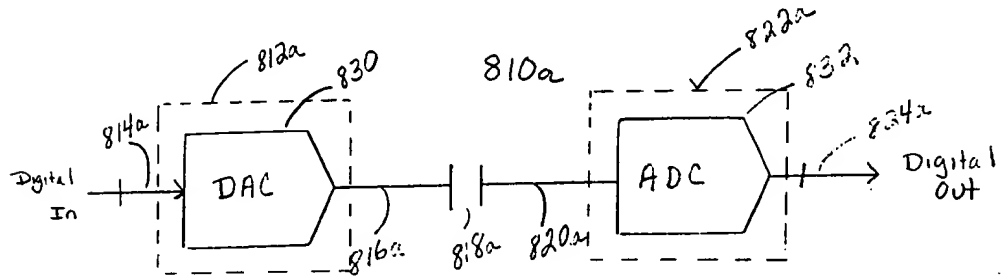

Fig. 22

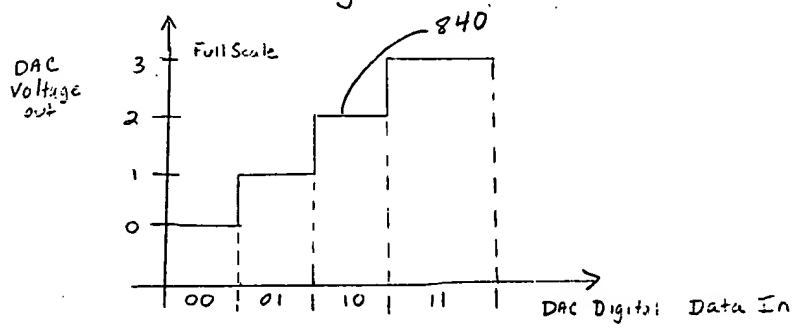

Fig. 23

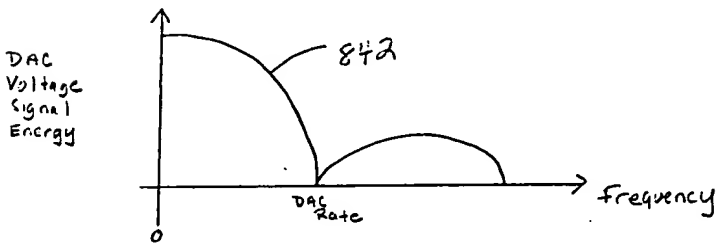

Fig. 24

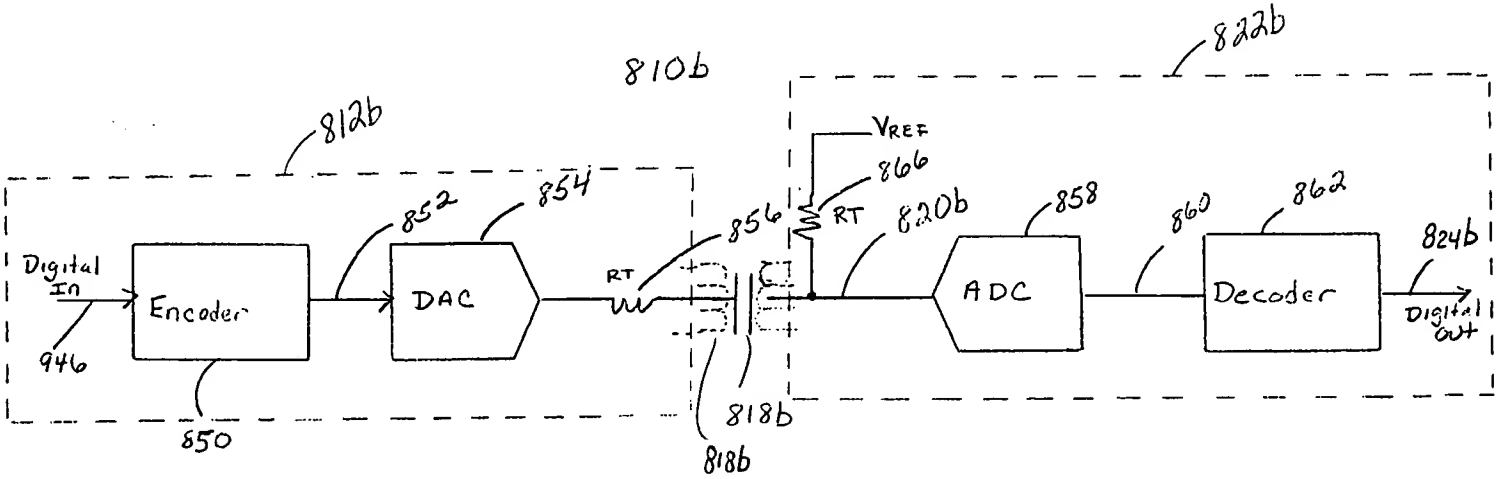

Fig 25

ENCODER

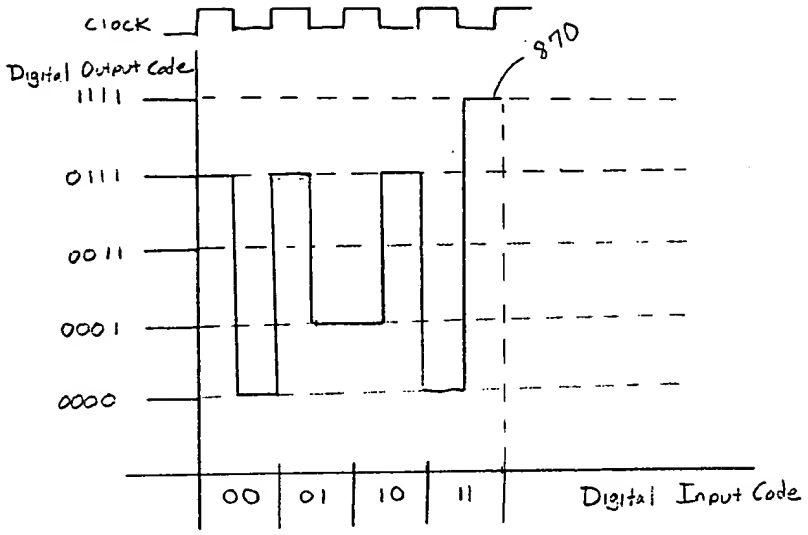

Fig 26

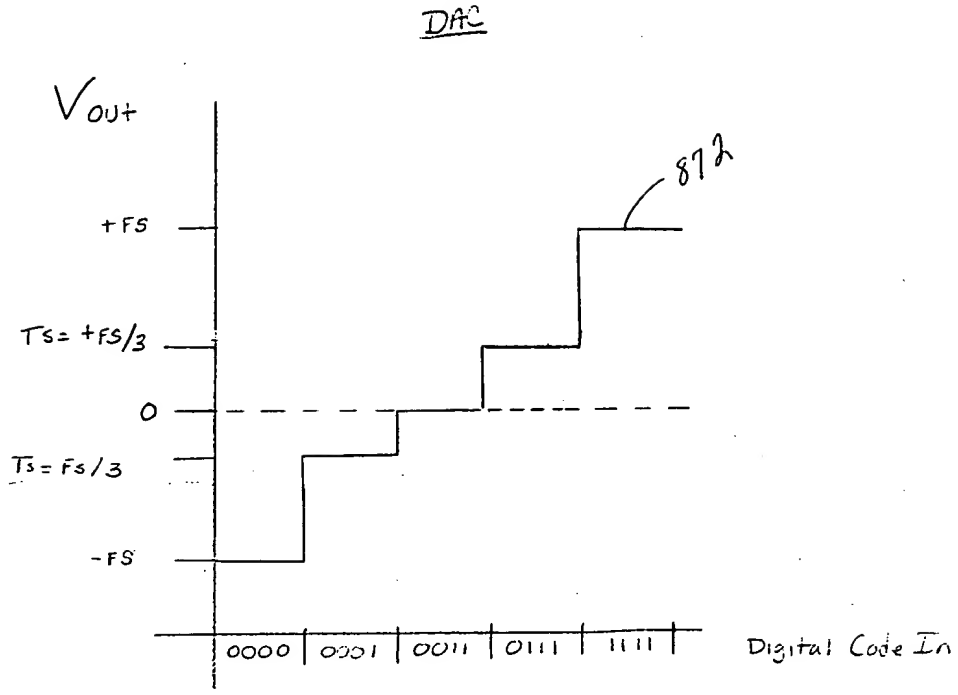
DAC
V_{OUT}
+FS
Ts= +FS/3
0
Ts = Fs/3
-FS
0000
0001
0011
0111
1111
Digital Code In
872

Fig. 27

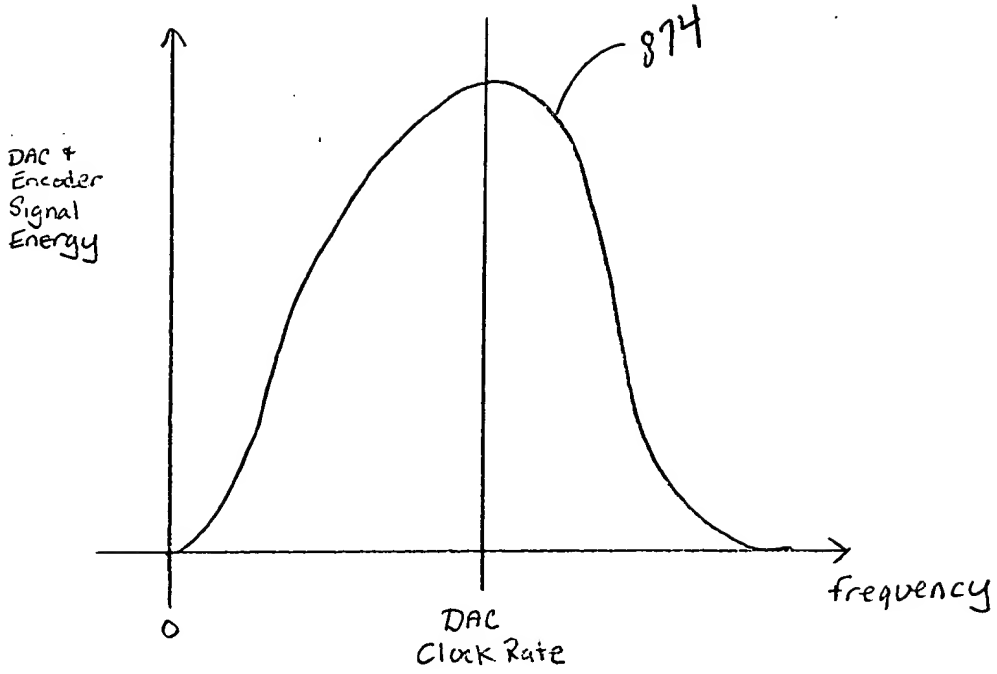

Fig. 28

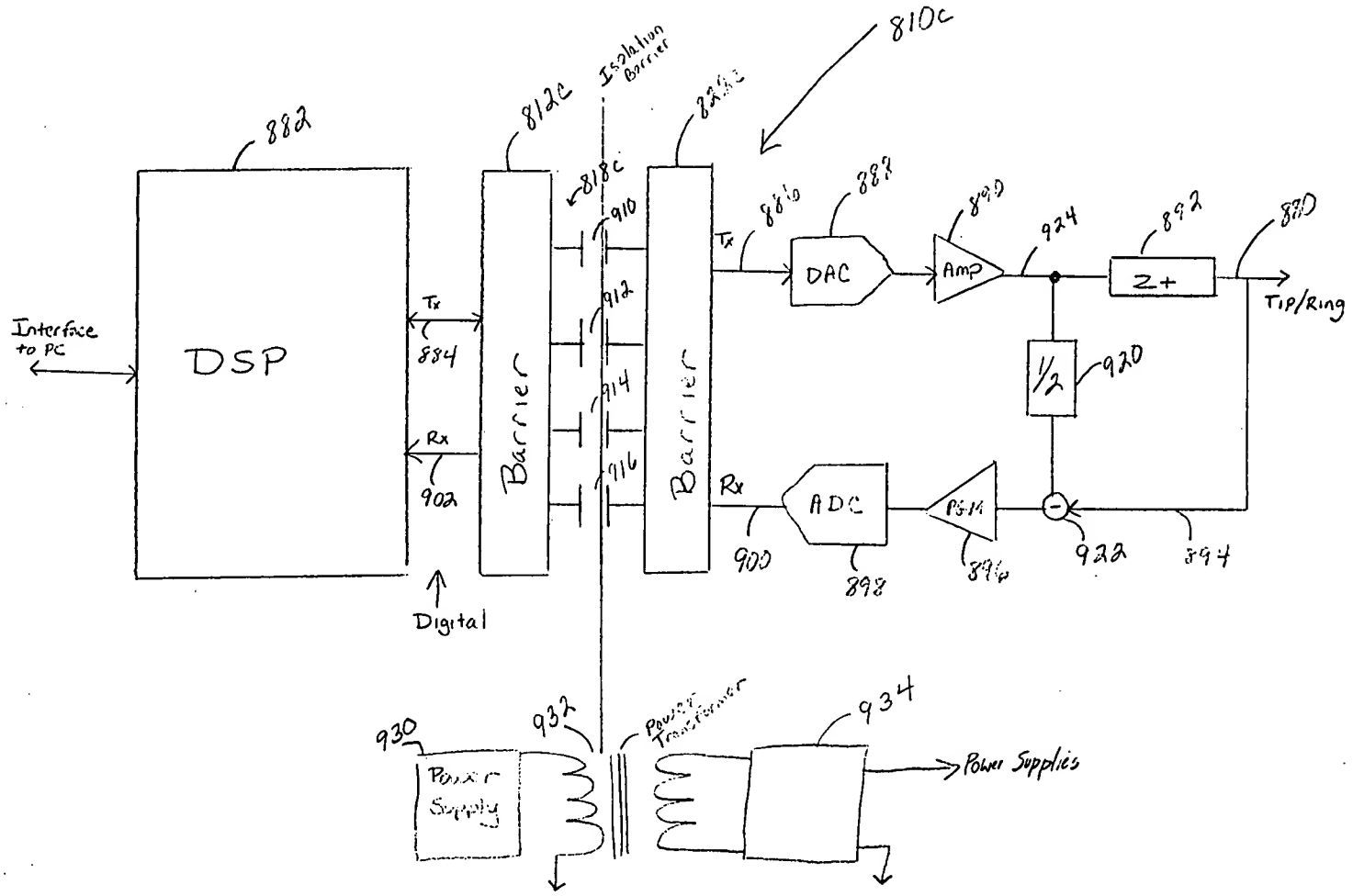

Fig. 29

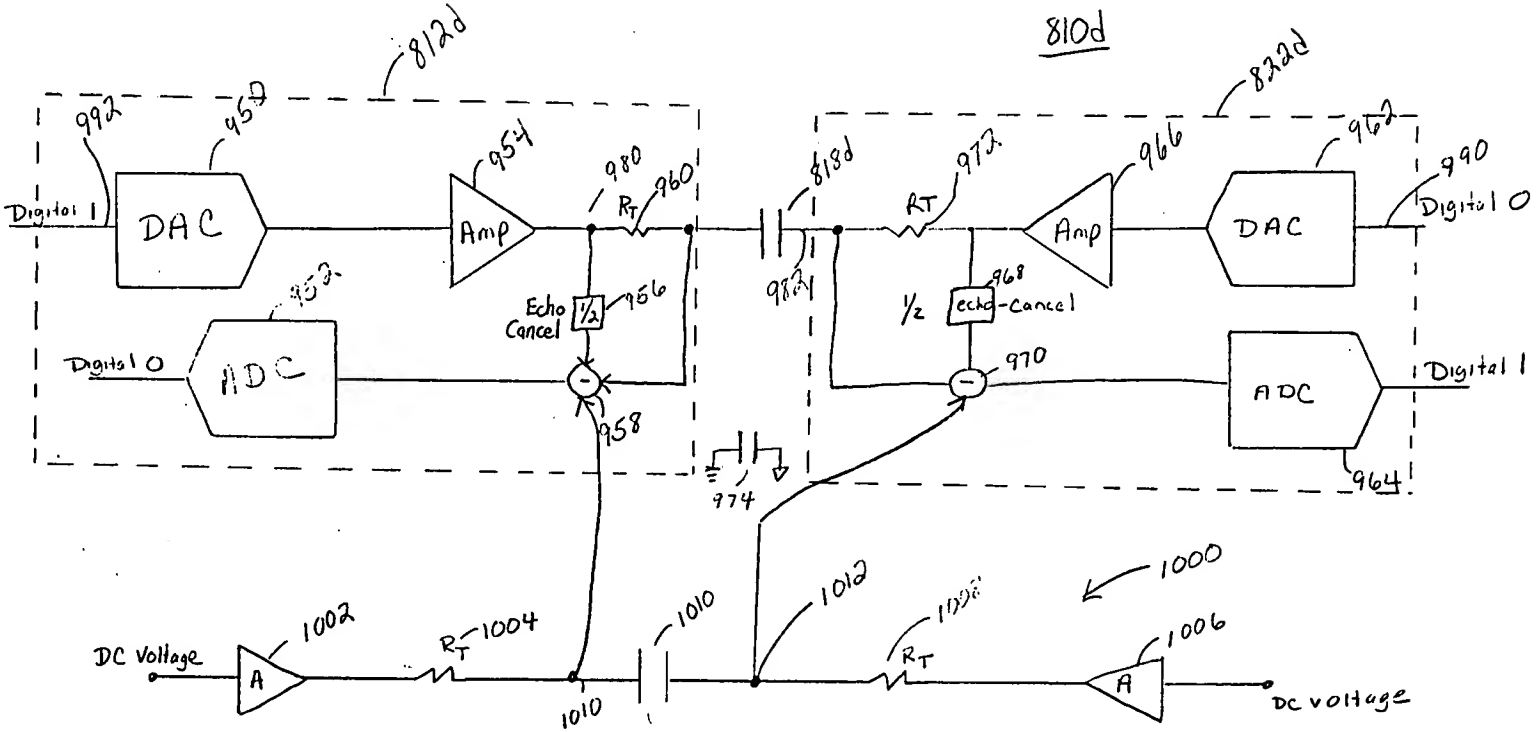

Fig 30

Full Barrier System 810e

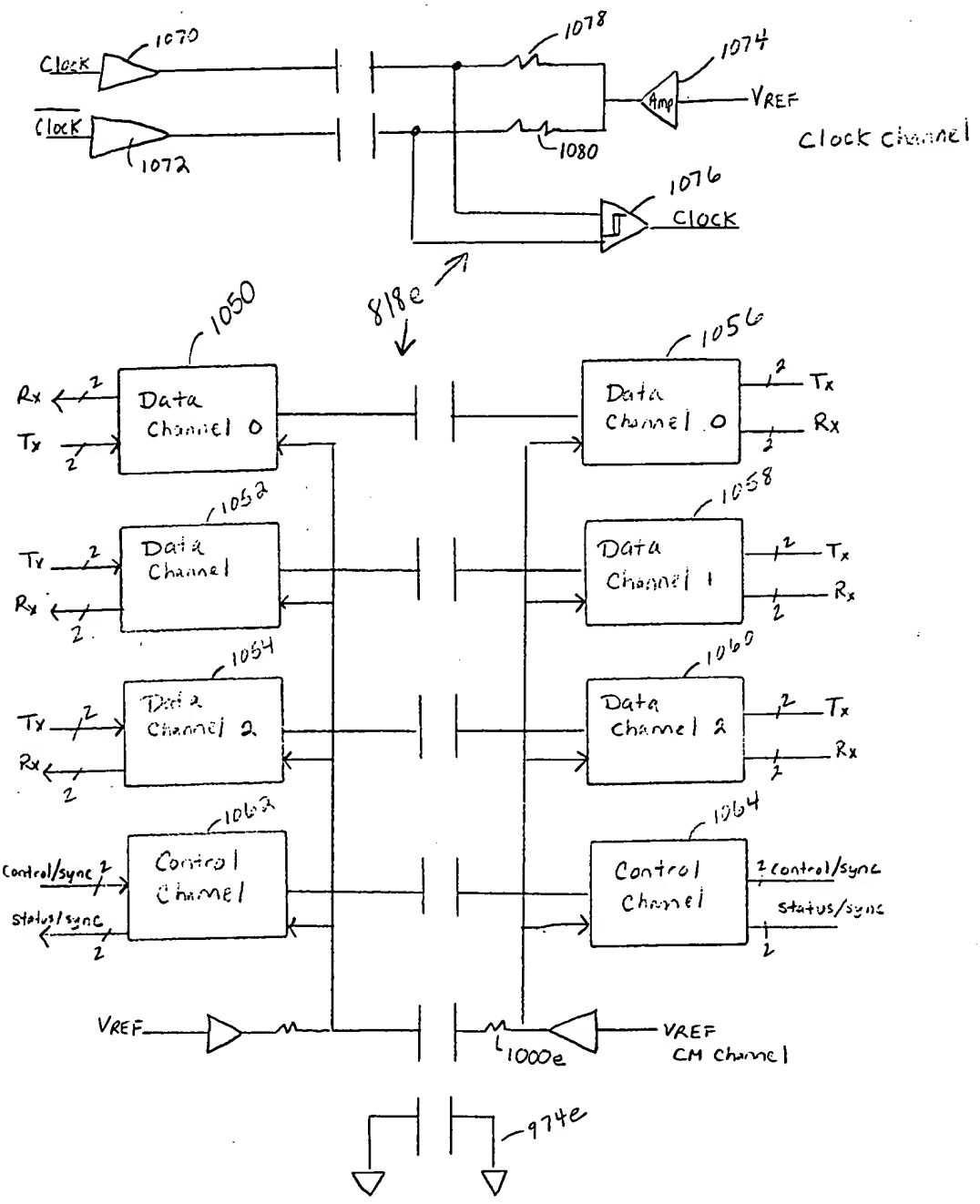

Fig. 31

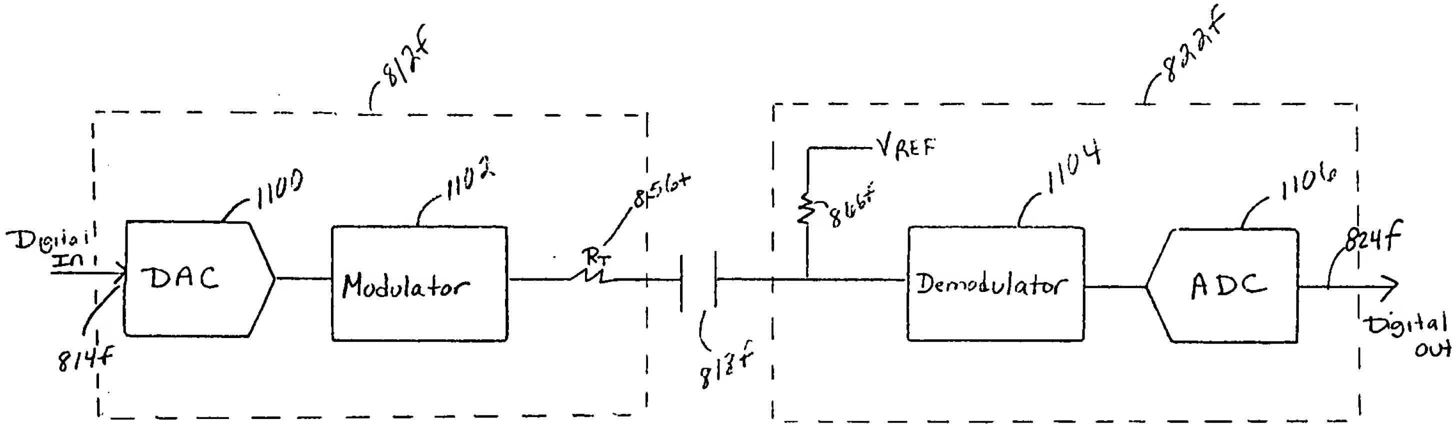

Fig. 32